UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,098	12/31/2003	Afshin Momtaz	51358/SDB/B600	9593

23363 7590 10/29/2004

CHRISTIE, PARKER & HALE, LLP
PO BOX 7068
PASADENA, CA 91109-7068

EXAMINER	
CHANG, DANIEL D	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 10/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,098	MOMTAZ ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *1-15 and 25-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16,23,24,29,31-35 and 38* is/are rejected.

7)☒ Claim(s) *17-22,30,36 and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Acknowledgement

Receipt is acknowledged of the Amendment filed October 8, 2004 with the election of Species of Fig. 7.

Claim Objections

Claim 19 is objected to because of the following typographical error: on line 2, "the logic circuit" appears to be --the write clock present detector--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 16, 23, 24, 29, 31-35, and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Traylor (US 5,473,756).

Regarding claim 16, Traylor discloses at least in Fig. 5A, a write clock present detector (as for the recitation, "write clock present detector", it is noted that "the PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art," *In re Morris*, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997).) for a first-in first-out (FIFO) circuit, the write clock present detector comprising:

a read shift register (501) having a first plurality of serially-coupled registers (502-504) and configured to shift a read flag signal (D in 502) in response to a read clock (518);

a write shift register (302) having a second plurality of serially-coupled registers (3 registers in 302) and configured to shift a write flag signal (D in first register in 302) in response to a write clock (516); and

a logic circuit (505-508, 520) coupled to an output of the read shift register (555) and an output of the write shift register (323), and configured to logically combine the write flag signal with the read flag signal to generate a write clock present detect output signal (521).

Regarding claim 29, Traylor discloses at least in Fig. 5A, that the write clock present detect output signal is generated (521) when the read and write flag signals propagate to the logic circuit (col. 8, lines 1+).

Regarding claim 23, Traylor discloses at least in Fig. 5A, a method of detecting the presence of a write clock (516) for a first-in first-out (FIFO) circuit, the method comprising:

propagating a read flag signal (D in 502) through a read shift register (502, 503) in response to a read clock (518);

propagating a write flag signal (D in first register in 302) through a write shift register (left 2 register in 302) in response to the write clock; and

comparing (col. 8, lines 1+) an output of the read shift register with an output of the write shift register to generate a write clock present output signal (521).

Regarding claim 24, Traylor discloses at least in Fig. 5A, periodically resetting (515, when resetting FIFO; col. 8, lines 17+) the read shift register and the write shift register.

Regarding claim 31, Traylor discloses at least in Fig. 5A, that the write clock present output signal (521) is generated when the read and write flag signals propagate to a logic circuit (505, 506, 508, 520).

Regarding claim 32, Traylor discloses at least in Fig. 5A, that the write clock present output signal is generated when the read and write flag signals propagate to a logic circuit (505, 506, 508, 520) before a reset (515; before next FIFO reset) occurs.

Regarding claim 33, Traylor discloses at least in Fig. 5A, delaying (508) the generation of the write clock present output signal after comparing (505, 506) the output of the read and write shift registers.

Regarding claim 34, Traylor discloses at least in Fig. 5A, further propagating the read flag signal through the read shift register (including 504) in response to the read clock to generate the write clock present output signal.

Regarding claim 35, Traylor discloses at least in Fig. 5A, clocking a register (504) with the further propagated (by 504) read flag signal to generate the write clock present output signal.

Regarding claim 38, Traylor discloses at least in Fig. 5A, initiating the propagation of the read flag signal and the write flag signal after generation of a reset signal (col. 8, lines 17+) for the read and write shift registers.

Allowable Subject Matter

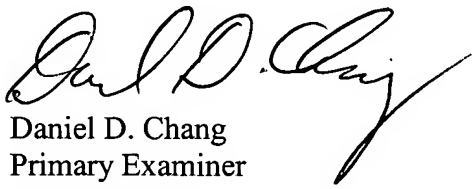
Claims 17-22, 30, 36, and 37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Daniel D. Chang
Primary Examiner
Art Unit 2819

dc

DANIEL CHANG
PRIMARY EXAMINER